CLAIMS

1. A method for generating an address value for addressing a memory (31), comprising the step of generating a plurality of address fragments, **characterized** by the step of:

comparing only a fraction of the generated address fragments with a maximum allowable value.

2. The method according to claim 1, wherein every second address fragment is compared.

3. The method according to claim 1 or 2, further comprising the steps of:

discarding the compared address fragment if it exceeds the maximum allowable value; and

accepting the compared address fragment otherwise.

4. The method according to any of the previous claims, further comprising the step of:

permuting the generated address fragments,

wherein the address fragments to be compared are permuted prior to or after the step of comparing.

5. The method according to any of the previous claims, further comprising the step of:

appending at least one bit being the most significant bit(s) to any address fragment or permuted address fragment

6. The method according to any of the previous claims, wherein the compared address fragment is an odd address fragment to which a 1 is to be appended as a most significant bit.

7. The method according to any of the previous claims, wherein an even address fragment is generated in

response to discarding or accepting the compared address fragment.

8. The method according to any of the claims 1 to 6, comprising the step of:

generating at least the odd address fragment to be compared and a following even address fragment during a first clock cycle;

if the compared odd address fragment is discarded, outputting the even address fragment during the first clock cycle;

if the compared odd address fragment is accepted, outputting the odd compared address fragment and retaining values of registers of a shift register during the first clock cycle; and

outputting the even address fragment during a second clock cycle following the first clock cycle.

9. The method according to any of the previous claims, comprising the step of:

generating a next odd address fragment; and

inputting the next odd address fragment into registers (120a-120d) of a shift register.

10. The method according to claim 8 or 9, wherein the next even and next odd address fragments are generated by means of a feedback function (g(x)).

11. A device (100, 200, 300) for generating address values for addressing a memory (31), comprising means (110a-110d, 140a, 140b) for generating a plurality of address fragments, **characterized** by

comparator means (160, 260, 360) adapted to compare only a fraction of the plurality of address fragments generated with a maximum allowable value.

12. The device according to claim 11, wherein the comparator is adapted to compare every second generated address fragment.

13. The device according to claim 11 or 12, further comprising selector means (150), which is adapted to discard the compared address fragment if it exceeds the maximum allowable value, and to accept the compared address fragment otherwise.

14. The device according to any of the claims 11 to 13, further comprising permuting means (130a, 130b) adapted to permute the address fragments, the permuting means being provided prior to or after the comparator means (160, 260, 360).

15. The device according to any of the claims 11 to 14, further comprising toggle means (170) adapted to append at least one bit being the most significant bit(s) to any address fragment, or permuted address fragment, in order to generate the address value.

16. The device according to any of the claims 10 to 13, wherein the compared address fragments are address fragments to which a 1 is to be appended as a most significant bit.

17. The device according to any of the claims 11 to 16, wherein the means (110a-110d, 140a) for generating address fragments is adapted to generate a next even address fragment in response to discarding or accepting the compared address fragment.

18. The device according to any of the claims 11 to 16, wherein the means for generating address fragments comprises:

a shift-register comprising a predetermined number of registers (110a-110d) adapted to generate address fragments to be compared during a first clock cycle,

address fragment calculation means (140) adapted to generate a next even address fragment during the first clock cycle, which is based on the address fragment to be compared;

the selector means (150) is adapted to, if the compared address fragment is discarded, output the even address fragment in response to a first control signal (M) during the first clock cycle, and to output the compared address fragment during the first clock cycle if the compared address fragment is accepted, and to output the even address fragment during a second clock cycle following the first clock cycle; and

the shift register is adapted to retain present values of the registers during the first clock cycle in response to a second control signal (E) if the compared address fragment is accepted.

19. The device according to claim 18, wherein the address fragment calculation unit means (140a, 140b) is adapted to generate a next odd address fragment, based on the even address fragment, and feed back said next odd address fragment to the shift register.

20. The device according to claim 18 or 19, wherein the address fragment calculation means (140a, 140b) is adapted to generate the next even and next odd address fragments by means of a feedback function.

21. The device according to any of the claims 11 to 20, wherein the device (100, 200, 300) is implemented by software comprising readable program means to be run by a processor.

22. The device according to any of the claims 11 to 20, wherein the device (100, 200, 300) is implemented as an application specific integrated circuit.

23. The device according to any of the claims 11 to 20, wherein the device (100, 200, 300) is implemented as a field programmable gate array.

24. The device according to any of the claims 11 to 23, further comprising a shift register adapted to generate a maximum length pseudo noise sequence.

25. The device according to any of the claims 11 to 24, wherein the memory (31) is an interleaver memory.

26. The device according to any of the claims 11 to 24, wherein the memory (31) is a deinterleaver memory.

27. An interleaver for interleaving a block of data, comprising a memory (31) and a device (100, 200, 300) for generating address values according to any of the claims 11 to 25 for addressing the memory.

28. A deinterleaver for interleaving a block of data, comprising a memory (31) and a device (100, 200, 300) for generating address values according to any of the claims 11 to 24 and 26 for addressing the memory.

29. A communication apparatus for communicating data, comprising a memory (31) and a device according to any of

the claims 11 to 26 for generating address values for addressing the memory.

30. The communication apparatus according to claim 29, wherein the communication apparatus is a mobile radio terminal, a pager, a communicator, an electronic organizer, or a smartphone.

31. The communication apparatus according to claim 29, wherein the communication apparatus is a mobile telephone (1).

32. A communication apparatus for receiving data, comprising a deinterleaver according to claim 28.

33. The communication apparatus according to claims 32, wherein the communication apparatus is a set-top-box, a TV-set, or a mobile television receiver.

34. A software program product embodied on a computer readable medium comprising instructions for carrying out the method according to any of the claims 1 to 10 when said product is run by a processor.